



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: DEBASHIS BHATTACHARYA et al.  
Serial No: 09/896,059  
For: METHOD FOR AUTOMATED DESIGN OF INTEGRATED  
CIRCUITS WITH TARGETED QUALITY OBJECTIVES  
USING DYNAMICALLY GENERATED BUILDING  
BLOCKS  
  
Filed: JUNE 29, 2001  
Examiner: THOMPSON, ANNETTE M.  
Art Unit: 2825  
Docket No.: 162.7107USU

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 2313-1450

9#/amd#a  
7/1/03  
RECEIVED  
JUL 8 2003  
TECHNICAL CENTER 2800

**AMENDMENT**

Dear Sir:

In response to the Office Action dated March 28, 2003, please enter and consider the following amendments and remarks in the above-noted application.

07/07/2003 SDENB0B1 00000022 09896059

01 FC:2201  
02 FC:2202

168.00 OP  
279.00 OP